REMARKS

The Office Action dated November 22, 2005 has been carefully considered. Claims 1-18 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1, 11, and 17-18 have been amended in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claim 18 stands objected to because of an informality. Accordingly, the word "to" has been deleted from Claim 18. Applicants contend that the rationale underlying this amendment bears no more than a tangential relation to any equivalence in question because Claim 18 merely contained a typographical error. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S.Ct. 1831 (2002).

Claims 1-3, 8, 11-13, and 17 stand rejected under 35 U.S.C. § 103(a) in view of U.S. Patent Publication No. 2002/0116181 to Khan et al. ("Khan") and U.S. Patent 6,611,920 to Fletcher et al. ("Fletcher"). Insofar as these rejections may be applied against the amended claims, they are deemed overcome.

Claim 1 has been amended to clarify a distinguishing feature of the present invention. The control logic of Claim 1 is at least configured to "generate an instruction-valid control bit, wherein *the at least one instruction-valid control bit is configured to enable the first clock and the second clock in response to a scan mode signal.*" Support for this amendment can be found, among other places, page 6, line 16 through page 7, line 9 of the original Application.

The Khan and Fletcher references do not teach, suggest, or disclose this feature of the present invention. Specifically, Khan discloses a digital signal processor with an integrated module configured to compute a Coordinate Rotation Digital Computer (CORDIC) in a pipeline. The pipelined module provides a CORDIC computation for each clock pulse. Fletcher discloses a

power control system for an integrated circuit that is integrated into a clocking system. This power control system can disable functional units within the integrated circuit when there are no valid instructions to be processed.

In contrast to the cited references, the present invention can enable the clocks within the microprocessor in response to a scan mode signal. A microprocessor is put into scan mode to facilitate testing of the logic within the microprocessor. Therefore, a scan mode signal can indicate that the microprocessor is being tested or is about to be tested. Normally, scan mode testing is accomplished by sending scan signals through specific portions of logic within the microprocessor and testing the outputs. During scan mode clocks enable the stages of logic so that the scan signals can stage through the logic of the microprocessor. The ability to enable the clocks of a microprocessor in response to a scan mode signal facilitates the scan mode testing of specific portions of logic within the microprocessor. This feature of the present invention is clearly not disclosed in the cited references.

In view of the foregoing, it is apparent that the cited references do not disclose, teach, or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is both clearly and precisely distinguishable over the cited references in a patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) in view of Khan and Fletcher be withdrawn and that amended Claim 1 be allowed.

Claims 2-3 and 8 depend upon and further limit amended Claim 1. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 2-3 and 8 also be withdrawn.

Claims 11 and 17 have been amended to clarify the same distinguishing feature as amended Claim 1. Hence, for at least the aforementioned reasons amended Claims 11 and 17 should also be deemed to be in condition for allowance. Specifically, the cited references do not disclose "*generating a scan mode signal, wherein in response to the scan mode signal, the instruction-valid control bit enables the first clock and the second clock.*" Accordingly, Applicants respectfully request that the rejection of Claims 11 and 17 under 35 U.S.C. § 103(a) in view of Khan and Fletcher be withdrawn and that amended Claims 11 and 17 be allowed.

Claims 12 and 13 depend upon and further limit amended Claim 11. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 12 and 13 also be withdrawn.

Claims 4-7, 9 and 14-16 stand rejected under 35 U.S.C. § 103(a) in view of Khan, Fletcher, and U.S. Patent 6,304,125 to Sutherland ("Sutherland"). Insofar as these rejections may be applied against the amended claims, they are deemed overcome. Claims 4-7 and 9 depend upon and further limit amended Claim 1. Claims 14-16 depend upon and further limit amended Claim 11. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 4-7, 9 and 14-16 be withdrawn.

Claim 10 stands rejected under 35 U.S.C. § 103(a) in view of Khan, Fletcher, and U.S. Patent 6,629,250 to Kopser et al. ("Kopser"). Insofar as this rejection may be applied against the amended claims, it is deemed overcome. Claim 10 depends upon and further limits amended Claim 1. Hence, for at least the aforementioned reasons, this Claim should be deemed to be in condition

for allowance. Accordingly, Applicants respectfully request that the rejection of dependent Claim 10 be withdrawn.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-18.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of Carr LLP.

Should the Examiner deem that any further amendment is desirable to place this Application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 2/22/06

CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3030
Fax: (214) 760-3003

Gregory W. Carr
Reg. No. 31,093